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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/275,502	03/24/99	DUGGIRALA S	SNSY-A1998-0

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EXAMINER	
SIEK, V	
ART UNIT	**PAPER NUMBER**
2825	5

DATE MAILED: 09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/275,502	Applicant(s) DUGGIRALA ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/275,502 and amendment filed on 7/3/2001. Claims 1-26 remain pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang et al (U.S. Patent No. 5.703.789) in view of Crouch et al (U.S. Patent No. 5,592,493).

4. As to claim 1, Beausang et al a computer implemented process and system for electronic design automation (EDA) (see abstract, col 1, lines 12-31), where the computer implemented process and system is used in design, checking, and testing of large scale integrated circuits. The process comprising receiving an HDL description of an integrated circuit (IC) design (Fig. 8, HDL description); generating a scannable netlist based on said HDL description, said scannable netlist comprising a scan chain (Fig. 8, scannable netlist contain scan chain; col 14, lines 56-59). Beausang et al teach that the test ready (TR) compiler can better optimize the overall layout for the additional of the test resources (see abstract). It is well known the art that a netlist is generated from HDL description of an IC design and a generated netlist is provided for placement and

routing tools in order to generate a layout of the IC design to meet timing and area specifications. Beausang et al does not teach partitioning the scan chain.

Crouch et al teach a process and system that provide a scan test architecture for use with a full-scan partitioned logic design implementation that can conduct scan tests at or above the rated frequency of the integrated circuit (IC) in such a manner that frequency dependent faults can be detected and isolated within any targeted partition block within the IC (col 2, lines 5-13, lines 44-65; Figs. 1-2). The scan test architecture comprising a partition scan chain (Fig. 1), where the partitioned scan chain comprising a plurality of sets of re-orderable scan cells (Fig. 2, set of partitioned scan chain 32, 34, and 36 by grouping scan cells based on respective clock domains; col 12, line 52 to col 13, line 34; where Fig. 14 shown detail process of re-orderable scan cells within each of the sets in order to obtain proper transition at E within a time period or a clock domain, and transition at P and all the path establishing values must also occur, but within the previous clock domain), wherein the partitioning information which describes the scan cells of each set is generated (Fig. 14 shown one of the partitioned scan chain information that describes the scan cells; col 12, lines 52 to col 13, line 61).

Crouch et al does not explicitly teach re-ordering scan cells of the scan chain during layout processes of the IC design, based on the partitioning information, by re-ordering only scan cells of a same set and not re-ordering scan cell of different sets. However, Crouch et al teach, in Fig. 14, that in order for the transition to occur at E within a clock domain, a transition must occur at P and all the path establishing values must also occur, but in the previous clock cycle domain to the expected transition (col

12, line 52 to col 13, line 50; Fig. 14). The path traversed point E is identified as critical path that must be met such timing condition. In order to preserve such clock cycle domains, re-ordering scan cells of the scan chain during layout processes of the IC design based on the partitioning information would have been necessary, where the re-ordering scan would have only performed of a same set and not of different sets since this would have preserved the clock cycle domains within the set of scan chain partitioned. Accordingly, integrating the teachings of partitioning scan chain as taught by Crouch as described above into Beausang's computer implemented process for EDA, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included re-ordering scan cells of the scan chain during layout processes of the IC design as claimed because, in this way, it would have improved IC design layout included scan chain, since this would have preserved timing conditions (clock cycle domains) of the partitioned scan cells within scan chain segments (set of partitioned scan cells), thereby the IC design layout included scan chain would have been obtained in accordance with the timing conditions as set forth in the partitioning scan chain. In addition, IC design verification using above process would have performed with more accuracy, thereby it would have enhanced the IC design included scan chain.

5. As to claims 2, 9 and 16, Crouch et al teach partitioning further comprising grouping scan cells of the scan chain into different sets based on the respective clock domains (Figs. 1, 2, 13 shown different sets of scan chains: examples partitioned blocks 32, 34 and 36 in Fig. 2; Fig. 14 shown detail of each set having groups of scan cells;

different sets based the respective clock domains described in col 12, line 52 to col 13, line 34).

6. As to claims 3, 10 and 17, Crouch et al teach partitioning further comprising grouping scan cells of the scan chain into set of rising-edge of the clock (col 12, lines 7-22). Crouch et al do not explicitly teach grouping scan cells of the scan chain into different sets based on their respective edge sensitivity types. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to group scan cells of the scan chain into different sets based on their respective edge sensitivity types as in Crouch's partitioning scan chain because, in this way, different sets of rising-edge of the clock and falling-edge of the clock would have provided more flexibility in IC design depending on design specifications.

7. As to claims 4, 11 and 18, Crouch et al teach partitioning further comprising grouping scan cells of the scan chain into different sets based on their respective positions in relation to a reconfiguration multiplexer of said scan chain (Figs. 1 and 13, dynamic scan chain remap MUX).

8. As to claims 5, 12 and 19, Crouch et al teach partitioning scan chain into groups of scan cells, where the groups of scan cells are designed within a microprocessor or any IC design device (Fig. 1, col 7, lines 5-24). Many types of scan cells exist in the art and Crouch et al also suggest that many scan architecture and methodologies exist in the art may be incorporated with his partitioning scan chain method (col 14, lines 6-15). Crouch et al teach that the clock (PCLK in Figs. 1 and 13) input signal is the functional system clock used to synchronize the updating of all sequential elements contained

within the IC device regardless of whether the device is in scan mode or functional mode (normal mode) (col 7, lines 49-53). It is noted that clock skew tolerance is well in the art and circuit designers used clock skew tolerance to optimize timing of IC design device. Crouch et al do not explicitly teach grouping scan cells of the scan chain into different sets based on their respective clock skew tolerance levels. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to group scan cells of the scan chain as shown in Figs. 1, 2, 13, 14 into different sets based on their respective clock skew tolerance levels because, based on these clock skew tolerance levels associated with each of the groups, circuit designers would have optimized timing delays within each group of the scan cells, thereby this would have improved the microprocessor or IC design device.

9. As to claims 6, 13 and 20, Crouch et al teach partitioning comprising grouping scan cells of the scan chain into different sets based on their respective surrounding cone logic (Fig. 14 shown cone logic from point E).

10. As to claims 7, 14 and 21, Crouch et al teach partitioning comprising grouping scan cells of the scan chain into different sets based on their respective output switching times (Fig. 14, switching times or transition times at P and E; col 12, line 52 to col 13, line 34).

11. As to claim 8, it is also rejected for the same reasons as set forth to rejecting claim 1 above, since claim 8 is merely a system for the method of operation defined in the method claim 1. In addition, although the cited reference do not explicitly teach reporting partitioning information indicative, it would have been obvious to one of

ordinary skill in the art at the time the invention was made because the reported partitioning information would have been necessary and used to provide to a placement and routing tool, thereby, based on the partitioning information, the IC layout would have been preserved timing specifications as set forth in the partitioning scan chain.

12. As to claim 15, it is also rejected for the same rationale as set forth to rejecting claim 1 above, since claim 11 is merely a computer system for the method of operation defined in the method claim 1. Beausang et al disclose a computer system comprising a processor coupled to a bus and a computer readable memory unit coupled to the bus, where the memory unit having a program stored therein causing the computer system to perform an electronic design automation (EDA) process (Fig. 2, col 5, line 34 to col 6, line 12). In addition, although the cited reference do not explicitly teach generating partitioning information indicative, it would have been obvious to one of ordinary skill in the art at the time the invention was made because the generated partitioning information would have been necessary and used to provide to a placement and routing tool, thereby, based on the partitioning information, the IC layout would have been preserved timing specifications as set forth in the partitioning scan chain.

13. As to claim 22, Beausang et al teach a method of constructing a scan chain comprising adding scan cells to a netlist description of an integrated circuit (IC) design, said scan cells being coupled serially together to form a first scan chan having a scan cell ordering (Fig. 8, where logic block 645 allocate resources to construct a scan chain between the scannable memory cells, thereby the memory cells are linked together to

create a scan chain, where a netlist is generated; col 14, lines 39-63). The scannable netlist is used for a layout of IC (see abstract).

Beausang et al do not explicitly teach partitioning scan cells of said first scan chain.

Crouch et al teach a process and system that provide a scan test architecture design for use with a full-scan partitioned logic design implementation that can conduct scan tests at or above the rated frequency of the integrated circuit (IC) in such a manner that frequency dependent faults can be detected and isolated within any targeted partition block within the IC (col 2, lines 5-13, lines 44-65; Figs. 1-2). The scan chain (first scan chain 32 in Fig. 2) is partitioned into sets of scan cells (Fig. 2, sets of scan cells 32, 34 and 36, where detail of each set is illustrated in Fig. 14). Crouch et al teach partitioning scan cells comprising grouping scan cells of the scan chain into different sets according to clock domains of said scan cells wherein scan cells of a given set share the same clock domain (Figs. 1, 2, 13 shown different sets of scan cells being grouped into first clock domain and second clock domain; partitioned blocks 32, 34 and 36 in Fig. 2; Fig. 14 shown detail of each set is grouped based on a different clock domain for example a first clock domain and second clock domain; col 12, line 52 to col 13, line 34). Crouch et al teach partitioning further comprising grouping scan cells of the scan chain into set of rising-edge of the clock (col 12, lines 7-22). This would have corresponded to partitioning scan cells into subsets according to edge sensitivity of said scan cells wherein scan cells of a given subset share the same edge sensitivity and the same clock domain (Fig. 14 shown signal along path 312 is based on a rising-edge of

clock, where scan cells of a given subset share the same clock domain; col 12, lines 7-22; col 12, line 52 to col 13, line 34). Crouch et al teach constructing a second scan chain (scan chain 34 in Fig. 2) by breaking said scan cell ordering of said first scan chain (breaking first scan chain 32 and second scan chain 34 by the partitioning scan chain of scan cells 96-86). Crouch et al do not explicitly teach reordering said scan cells based on said partitioning information wherein only scan cells of a same set are allowed to be reordered. However, Crouch et al teach, in Fig. 14, that in order for the transition to occur at E within a clock domain, a transition must occur at P and all the path establishing values must also occur, but in the previous clock cycle domain to the expected transition (col 12, line 52 to col 13, line 50; Fig. 14). The path traversed E is identified as critical path and timing path must be met a timing constraint. In order to preserve such timing constraint, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have generated partitioning information indicative from the partitioning scan as taught by Crouch above, and re-ordered scan cells based on the partitioning information wherein only scan cells of a same set are allowed to be reordered because, in this way, each of the partitioned sets of the scan chain would have constructed and verified in isolation with accuracy, since each of the sets of the scan chain would have been optimized in isolation. Thus, this would be a cost effective, since specific partitioned scan cells would have optimized in accordance with their design specifications.

Accordingly, integrating the teachings of partitioning scan chain as taught by Crouch as described above into Beausang's method of constructing a scan chain, it

would have been obvious to one of ordinary skill in the art at the time the invention was made the claimed invention, because, in this way, each of the partitioned sets of the scan chain would have constructed and verified in isolation with accuracy, since each of the sets of the scan chain would have been optimized in isolation. Thus, this would be a cost effective, since specific partitioned scan cells would have optimized in isolation in accordance with their design specifications.

14. As to claim 23, Beausang et al teach the scannable netlist is used for a layout of IC design (see abstract), where the layout includes placing and routing processes. Crouch et al do not explicitly teach constructing a second scan chain is performed during placing and routing processes performed on said netlist description. However, integrating the teachings of Crouch as described above into constructing of a scan chain as taught by Beausang, it would have been obvious to one of ordinary skill in the art at the time the invention was made the claimed invention because, in this way, each of the sets the scan cells would have placed and routed, then optimized based on the clock domain and edge sensitivity of the scan cells. Thus, this would have improved IC design, since each of the partitioned scan cells would have optimized in isolation to meet their design specifications.

15. As to claim 24, Crouch et al teach partitioning scan cells into subsets according to relative positions of the scan cells to a reconfigurable multiplexer of the first scan chain wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same relative position to the reconfigurable multiplexer (Fig. 2,

MUX 24 is corresponding a reconfigurable multiplexer; Fig. 14 shown the scan cells of the set share the same edge sensitivity (rising-edge) and the clock domain).

16. As to claim 25, Crouch et al teach partitioning scan cells into subsets according to respective surrounding cone logic of the scan chains wherein scan cells of a given subset share the edge sensitivity, the same clock domain and the same surrounding cone logic (Fig. 14 shown sharing the same cone logic from point E, the same clock domain at E, the same edge sensitivity of rising clock).

17. As to claim 26, , Crouch et al teach partitioning scan cells into subsets according to respective switching times (transition times at P and E) of the scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain logic (Fig. 14 shown sharing the same cone logic from point E, the same clock domain at E, the same edge sensitivity of rising clock) except for sharing the same power rail. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the partitioned scan cells as taught by Crouch would have shared the same power rail because this would be cost effective by using less IC area, thereby the same clock PCLK is provided to all flip-flops in the chip (Figs. 1, 13).

Remarks

18. Applicants argued that Crouch et al teach "clock cycle domain" or "clock domain", where clock domain is different from the clock domain as claimed. However, examiner see no differences found in the claims per broad interpretation by examiner. It is noted

that examiner examines the claims not the specification. Accordingly, the clock domain taught by Crouch corresponding to the clock domain as claimed.

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

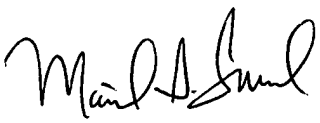
Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek
Art Unit 2825
September 13, 2001



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